



SYLVANIA

INTEGRATED CIRCUITS

Tentative Data

SUHL* II

*Sylvania Universal High-Level Logic.

SATURATED (40 mc/s) TTL CIRCUITS

Silicon Monolithic Epitaxial

MILITARY TEMP. RANGE -55°C to +125°C

INDUSTRIAL TEMP. RANGE 0°C to +75°C

August 6, 1965

DESCRIPTION:

SUHL * II is a family of TTL saturated digital logic circuits, consisting of totally compatible 6 nsec t_{pd} (typ) gates and 30 mc J-K flip-flops.

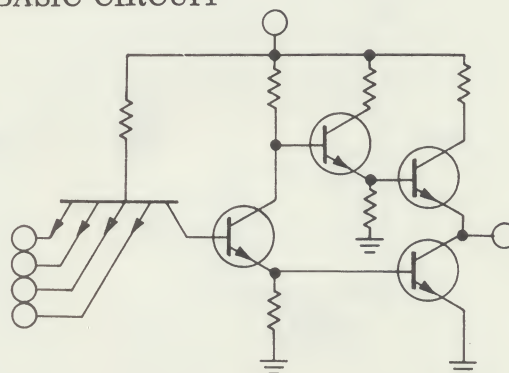
All circuits are characterized by high logic swing, noise immunity, and nominal capacitance drive at low power. SUHL * II operates from a single 5.0 volt power supply. SUHL II circuits are compatible with and can be intermixed with SUHL (I) circuits.

Circuit types are supplied in standard 14 lead flat package and 14 lead plug-in package.

FUNCTION

Expandable Dual 4-Input OR Gate	SG210 Series
Quad 2-Input NAND/NOR Gate	SG220 Series
Quad 2-Input OR Expander	SG230 Series
Dual 4-Input NAND/NOR Gate	SG240 Series
Expandable Quad 2-Input OR Gate	SG250 Series
Single 8-Input NAND/NOR Gate	SG260 Series
Dual 4-Input OR Expander	SG270 Series
J-K Flip-Flop (AND Inputs)	SF250 Series
J-K Flip-Flop (OR Inputs)	SF260 Series

BASIC CIRCUIT



CHARACTERISTIC SUMMARY:

1. High Speed TTL saturated logic;
2. High Noise Immunity;
3. High Logic Swing;
4. Low Power;
5. Low output impedance in the "0" and "1" level reduces noise pickup.
6. Single 5 volt power supply.
7. Low power OR expansion without fan-out degradation or capacitive loading of the gate output.
8. No complex loading rules since inputs and outputs are isolated.
9. Two operating temperature ranges:

Military	-55°C to +125°C
Industrial	0°C to +75°C
10. High fan-out;
11. Short circuit protection
12. Compatible with and can be intermixed with SUHL (1) circuits.

6 nsec gates, 30 mc J-K Flip Flops
 typically +1 volt, -1.5 volts, @25°C
 logic "0" = 0.25 volts, logic "1" = 3.5 volts
 typically 22 mw per gate function; 55 mw flip-flops
 independent of fan-in and fan-out

Fan-out of 5 to 12 similar gate loads.

This extension of SUHL to the 6 nsec range offers to the logic designer a saturated integrated circuit with the combined advantages of speed at low power, high reliability and a high degree of logic flexibility. The result is a digital logic family that facilitates complete system designs without compromising system performance.

$$L = (A \cdot B \cdot C \cdot N) + (E \cdot F \cdot G \cdot H) + \dots$$

$$\begin{array}{ll} C = \overline{A \cdot B} & K = \overline{H \cdot I} \\ G = \overline{E \cdot F} & N = \overline{L \cdot M} \end{array}$$

SG-230
SG-231
SG-232
SG-233

$$\begin{array}{l} L = \overline{A \cdot B \cdot C \cdot M} \\ K = \overline{E \cdot F \cdot G \cdot I} \end{array}$$

$$K = A \cdot N + C \cdot B + E \cdot F + G \cdot H \cdot I$$

SG-260
SG-261
SG-262
SG-263

SG-270
SG-271
SG-272
SG-273

$$Q_{n+1} = J_1 \cdot J_2 \cdot J_3 \cdot \bar{Q}_n + \overline{K_1 \cdot K_2 \cdot K_3} \cdot Q_n$$

$$Q_{n+1} = (J_1 \cdot J_2 + L_1 L_2) \cdot Q_n + (K_1 \cdot K_2 + M_1 \cdot M_2) \cdot Q_1$$

GENERAL CHARACTERISTICS (+ 25°C, 5.0 volts)

Ratings:

Operating Temperature

Storage Temperature

Military
-55°C to +125°C
-65°C to +200°C

Industrial
0°C to +75°C
-65°C to +200°C

Input Characteristics:

	Min.	Typ.	Max.	Unit
Logic "1" Voltage	1.7		5.5	volts
Logic "1" Current		30	200	μ a
Logic "0" Voltage			1.1	volts
Logic "0" Current		1.7	2.0 (MIL) 2.5 (Ind)	ma
Capacitance		1.5		pf
Positive Noise Immunity ¹		1.0		volts
Negative Noise Immunity		1.5		volts

Output Characteristics:

Logic "1" Voltage ²	3.0	3.5		volts
Logic "0" Voltage ³		0.25	0.45	volts
Propagation Delay Time/Gate (varies with circuit)		6	10	ns

Fan-out varies with circuit, designed for fan-outs of 5 to 12

1. Noise immunity is that voltage superimposed on the input which will not propagate beyond the following stage.
2. With max logic "0" output on input.
3. Prime at 20 ma, standard at 10 ma.

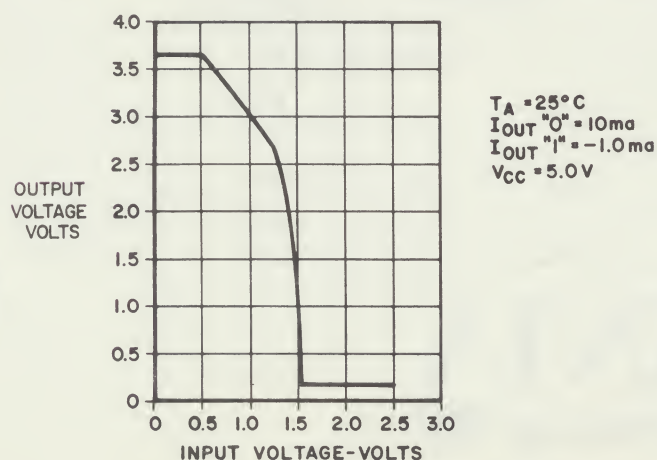
TYPICAL CHARACTERISTICS FOR CIRCUIT TYPES (+ 25°C, + 5.0 volts):

Function	Type Nos.	t_{pd} (nsec)	Avg. Power (mw)	Military (-55°C to +125°C)		Industrial (0°C to +75°C)	
				Prime F0	Std F0	Prime F0	Std F0
Expandable Dual 4-Input OR Gate	SG210, SG211, SG212, SG213	7	30	12	6	10	5
Quad 2-Input NAND/NOR Gate	SG220, SG221, SG222, SG223	6	22***	12	6	10	5
Quad 2-Input OR Expander	SG230, SG231, SG232, SG233	2	28				
Dual 4-Input NAND/NOR Gate	SG240, SG241, SG242, SG243	6	22***	12	6	10	5
Expandable Quad 2-Input OR Gate	SG250, SG251, SG252, SG253	7.5	43	12	6	10	5
Single 8-Input NAND/NOR Gate	SG260, SG261, SG262, SG263	8	22	12	6	10	5
Dual 4-Input OR Expander	SG270, SG271, SG272, SG273	2	6.7				
J-K Flip-Flop (AND Inputs)	SF250, SF251, SF252, SF253	30mc**	55	12	6	10	5
J-K Flip-Flop (OR Inputs)	SF260, SF261, SF262, SF263	30mc**	55	12	6	10	5

**Synchronous clock rate

*** Per gate

TYPICAL SUHL II TRANSFER CHARACTERISTICS:

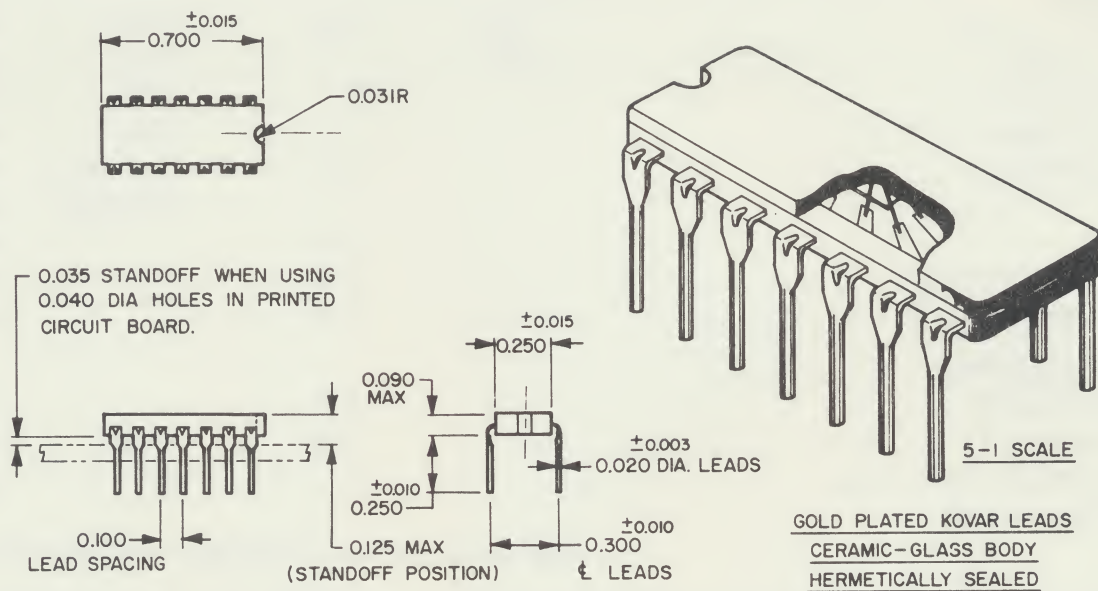


For electrical characteristics test methods and typical switching time variations vs. temperature, fan-out, and capacitance (up to 50pf) refer to corresponding SUHL (I) data sheets.

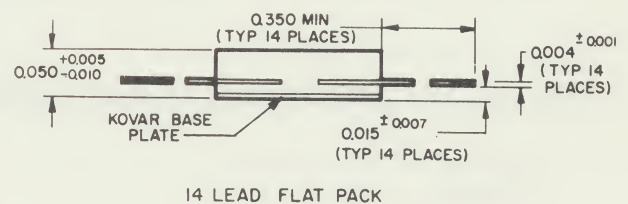
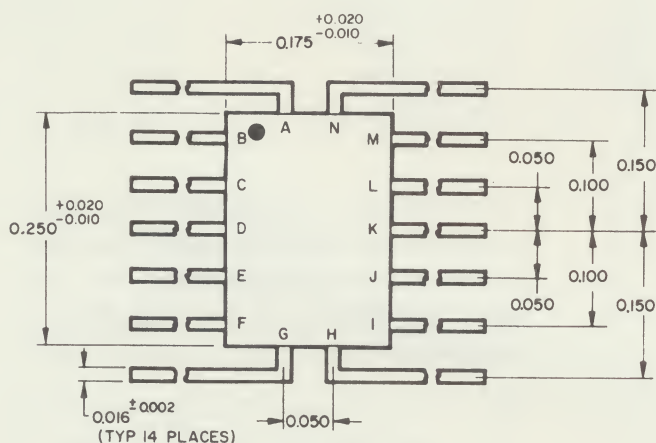
For reliability and quality assurance test conditions and methods refer to Sylvania specification "GTS 184".

Circuits may be ordered in standard flat package (50mil lead centers) by adding "02" suffix to the basic part number; in plug-in package (100mil lead centers) by adding "03" suffix to the basic part number.

14 LEAD PLUG-IN PACKAGE



- * Specifically designed for low cost assembly on two-sided printed circuit boards.
- * Leads are in a dual in-line arrangement.
- * 100 mil pin centers permit both loose drill tolerances and wide printed circuit lines.
- * Leads provide up to .035" standoff to prevent solder bridging.
- * Hermetically sealed and tested to 10^{-8} cc/sec leak rate.
- * Alumina filled glass package provides extremely low thermal resistance.
- * Index notch midway in one of the short sides to facilitate manual or automatic installation.
- * Kovar leads formed into a 0.020" diameter for both strength and reliable solderability.
- * Designed for dip or flow soldering attachment (63/37 solder at +275°C approx.).



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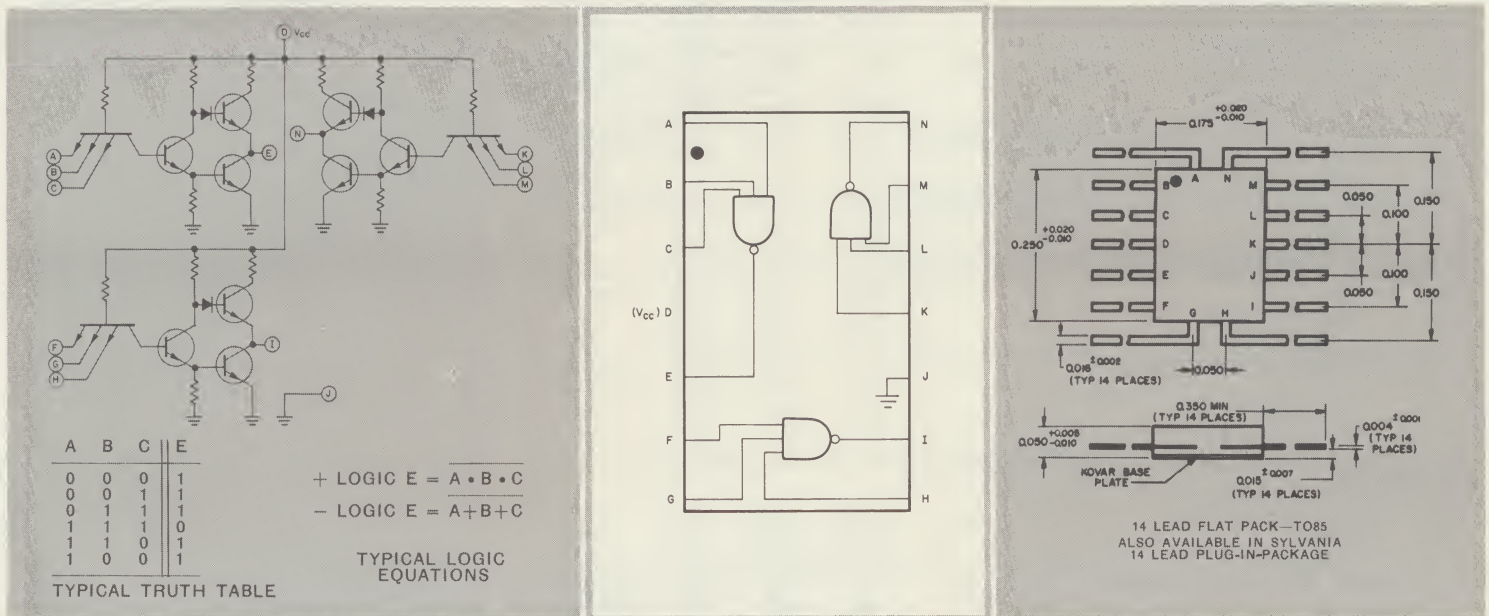
SYLVANIA

INTEGRATED CIRCUITS SUHL*

Triple 3-Input NAND/NOR Gate

SG190/SG191

Monolithic Silicon Epitaxial Circuit For Military Temp. Range -55°C to +125°C



CIRCUIT DESCRIPTION

The **SG 190** and **SG 191**, triple gates, are members of the SUHL* family of logic elements, which is a monolithic, epitaxial, saturated high speed logic family. Each package contains three gates consisting of a three-input AND gate followed by an inverting amplifier. Each of the gates functions as a NAND element in positive logic (as a NOR element in negative logic). These types are useful where multiple inverting functions are needed or where multiple drivers with fan outs up to 15 are needed such as in clock distribution systems. The circuit is designed for high speed operation over the temperature range of -55°C to +125°C without sacrificing characteristics of fan out, logic swing, noise immunity and capacitance drive at low power.

The circuit, requiring only a single power supply, has the following outstanding features:

CHARACTERISTIC SUMMARY

1. High fan out: 15 min. for **SG 190**; 7 min. for **SG 191**.
2. High speed: designed to operate at 20 mc, propagation delay time typically 10 nsec.
3. High noise immunity: ± 900 mV at 25°C at worst case fan out;
 ± 450 mV from -55°C to +125°C at worst case fan out.
4. High capacitance drive: up to 600 pf.
5. High logic swing: logic 0 is typically 0.26 volts;
logic 1 is typically 3.3 volts at 25°C.
6. Short circuit protection.
7. Low power: 15 mw average dissipation per gate.
8. Low output impedance in the 0 and 1 level reduces noise pickup.
9. No complex loading rules since input and output are isolated.

These features offer to the logic designer for the first time in an integrated circuit the combined advantages of speed at low power, high reliability and a high degree of logic flexibility. The result is a digital element that facilitates system design when combined with other SUHL elements.

* Sylvania Universal High level Logic

Electronic Components Group / SEMICONDUCTOR DIVISION / WOBURN, MASS.

November 1, 1965

RATINGS

Min. Typical Max.

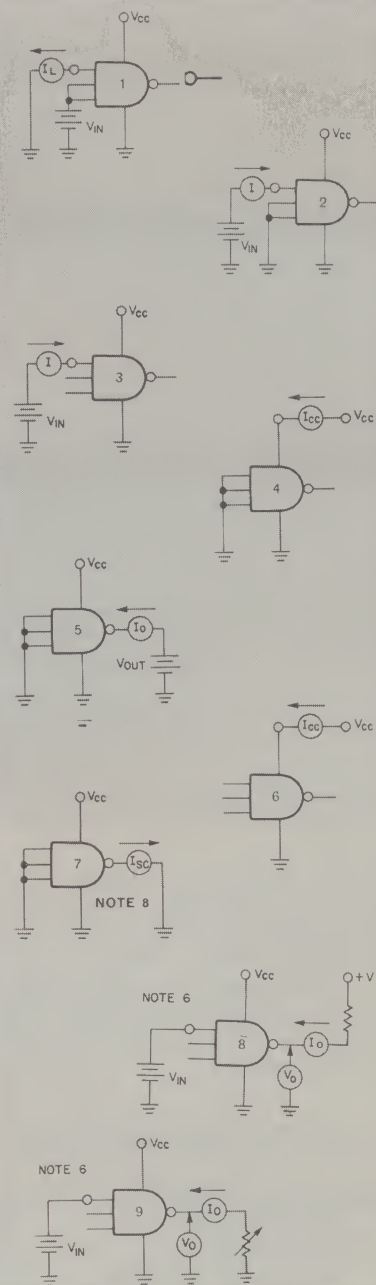
Min. Typical Max.

VOLTAGE			TEMPERATURE AND POWER		
Supply voltage (D.C.)		8.0 V _{DC}	Operating	-55	+125°C
Supply voltage (surge, 1 sec)		12.0 V	Storage	-65	+200°C
Supply voltage (operating)	4.5	5.0	Thermal gradient, junction to air (θ_{ja})		0.3°C/MW
Input voltage		5.5 V	Thermal gradient, junction to case (θ_{jc})		0.1°C/MW
Output voltage		5.5 V	Power Dissipation per gate (50% Duty Cycle, V _{CC} = +5v)	15	MW

ELECTRICAL CHARACTERISTICS

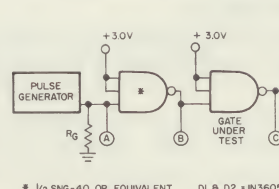
Characteristics at V _{CC} = +5.0V		Values at Required Temperatures			Units
Symbol		-55°C	+25°C	+125°C	
INPUT:					
Input Load Current @ V _{IN} = Other Inputs	I _L	1.33 0 +4.5	1.33 0 +4.5	1.33 0 +4.5	mA Max. Volts Volts
Input Leakage Current @ V _{IN} = Other Inputs	I _{IN LK}	0.1 +4.5 0	0.1 +4.5 0	0.1 +4.5 0	mA Max. Volts Volts
Inverse Beta Current @ V _{IN} = Other Inputs	B _{INV}	0.1 +4.5 Open	0.1 +4.5 Open	0.1 +4.5 Open	mA Max. Volts Volts
Input (OFF Level) Breakdown Voltage @ I _{IN} = Other Inputs	BV _{IN} "1"	+5.5 1.0 0	+5.5 1.0 0	+5.5 1.0 0	Volts Min. mA Volts
Input (ON Level) Breakdown Voltage @ I _{IN} = Other Inputs	BV _{IN} "0"	+5.5 1.0 Open	+5.5 1.0 Open	+5.5 1.0 Open	Volts Min. mA mA
Logic "1" Threshold Voltage V _{OUT} = I _{OUT} (SG-190) I _{OUT} (SG-191)	V _{TH} "1"	2.0 0.45 +20 10	1.7 0.45 +20 10	1.4 0.45 +20 10	Volts Volts Max. mA mA
Logic "0" Threshold Voltage V _{OUT} = I _{OUT} (SG-190) I _{OUT} (SG-191)	V _{TH} "0"	1.0 2.5 1.5 0.7	1.2 2.4 1.5 0.7	0.9 2.7 1.5 0.7	Volts Volts Min. mA mA
OUTPUT:					
Output Leakage Current @ V _{OUT} = Inputs	I _{O LK}	0.25 +5.5 0	0.25 +5.5 0	0.25 +5.5 0	mA Max. Volts Volts
Output Short Circuit Current @ Input	I _{SC}	10 45 0	10 45 0	10 45 0	mA Min. mA Max. Volts
Logic "0" Level @ V _{IN} = I _{OUT} (SG-190) I _{OUT} (SG-191)	Logic "0"	0.4 2.8 +20 10	0.4 2.8 +20 10	0.45 2.8 +20 10	Volts Max. Volts mA mA
Logic "1" Level @ V _{IN} = I _{OUT} (SG-190) I _{OUT} (SG-191)	Logic "1"	2.8 0.45 1.5 0.7	3.2 0.45 1.5 0.7	3.35 0.45 1.5 0.7	Volts Min. Volts mA mA
POWER REQUIREMENTS:					
Breakdown Voltage @ I _{CC} = Inputs	BV		+8.0 15 0		Volts Min. mA Volts
"ON" State Current Drain Inputs	I _{CC 0}	18 Open	18 Open	18 Open	mA Max.
"OFF" State Current Drain Inputs	I _{CC 1}	9 0	9 0	9 0	mA Max. Volts

Fig. No.



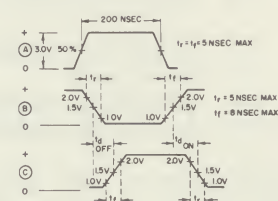
SWITCHING

SWITCHING CHARACTERISTICS	CONDITIONS		LIMITS	
	V _{CC} volts	T _A °C	FANOUT	TIME — nsec
			SG190	SG191
Turn On Delay	+5.0	+25	15	7
Turn Off Delay			15	7
Rise Time NOTE 7			15	7
Fall Time NOTE 7			15	7



* 1/2 SNG-40 OR EQUIVALENT DI 8 D2 = IN3605

NOTE:
(1) AVERAGE PROPAGATION TIME, $T_{pd} = \frac{t_{d ON} + t_{d OFF}}{2}$
(2) PULSE GENERATOR SKL 503 WITH RG-9 CABLE OR EQUIVALENT R_G ACCORDING TO GENERATOR USED.
(3) SCOPE RISE TIME ≤ 1 NSEC PROBE ≤ 5 pfd
(4) C_T = TOTAL CAPACITANCE TO INCLUDE STRAY WIRING + PROBE + LOAD
(5) R_L = 260Ω FOR SG-190, R_L = 570Ω FOR SG-191
(6) INPUTS ON OTHER GATES ARE GROUNDED.
(7) TO USE VOLTAGE REFERENCE, EXCHANGE RISE AND FALL TERMINOLOGY.
(8) ONLY ONE OUTPUT AT A TIME



See SG140/SG141 for characteristic curves.

11/1/65

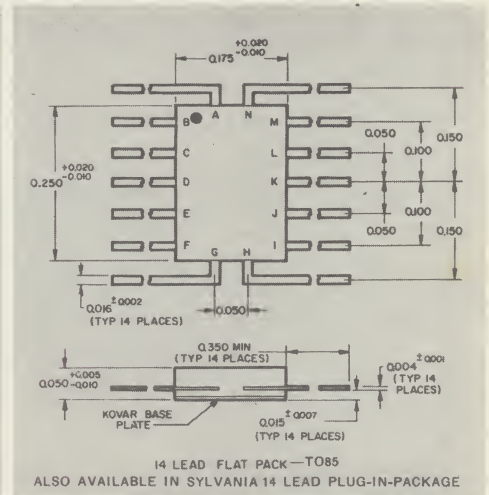
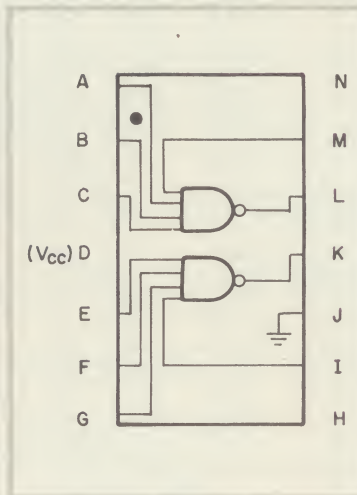
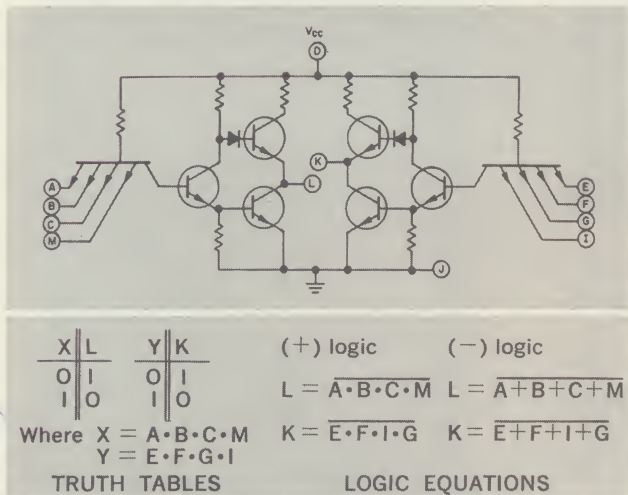
SYLVANIA

INTEGRATED CIRCUITS SUHL*

Dual Four Input NAND/NOR Gate

SG40/SG41

Monolithic Silicon Epitaxial Circuit For Military Temp. Range -55°C to +125°C



CIRCUIT DESCRIPTION:

The SG 40 and SG 41, Dual gates, are members of the SUHL* family of logic, which is a monolithic, epitaxial, saturated high speed logic family. Each package contains two gates, each consisting of a four input AND gate followed by an inverting amplifier. Each of the dual gates functions as a NAND element in positive logic (as a NOR element in negative logic) or, when cross coupled, as a set-reset flip-flop. The circuit is designed for high speed operation over the temperature range of -55°C to +125°C for military applications without sacrificing characteristics of fan out, logic swing, noise immunity and capacitance drive at low power.

This circuit, requiring only a single power supply, has the following outstanding features:

CHARACTERISTIC SUMMARY:

- | | |
|--|--|
| 1. High fanout: | 15 min for SG40 ; 7 min for SG41 |
| 2. High speed: | Designed to operate at 20 Mc, propagation delay time typically 10 nsec. |
| 3. High Noise immunity: | ± 900 Mv at 25°C and worst case fan out
± 450 Mv from -55°C to +125°C at worst case fan out
± 600 Mv from 0°C to +75°C at worst case fan out |
| 4. High capacitance drive: | Up to 600 pf |
| 5. High logic swing: | Logic 0 is typically 0.26 volts, Logic 1 is typically 3.3 volts at 25°C |
| 6. Short circuit protection: | |
| 7. Low power: | 15 mw avg. dissipation per gate. |
| 8. Low output impedance in the 0 and 1 level reduces noise pickup. | |
| 9. No complex loading rules since input and output are isolated. | |

These features offer to the logic designer for the first time in an integrated circuit the combined advantages of speed at low power, high reliability and a high degree of logic flexibility. The result is a digital element that facilitates system design when combined with other SUHL elements.

* Sylvania Universal High level Logic

Electronic Components Group / SEMICONDUCTOR DIVISION / WOBURN, MASS.

November 1, 1965

RATINGS

Min. Typical Max.

Min. Typical

Max.

VOLTAGE				TEMPERATURE AND POWER			
Supply voltage (D.C.)			8.0 V _{DC}	Operating	-55		+125°C
Supply voltage (surge, 1 sec)			12.0 V	Storage	-65		+200°C
Supply voltage (operating)	4.5	5.0	6.0 V	Thermal gradient, junction to air (θ_{ja})			0.3°C/MW
Input voltage			5.5 V	Thermal gradient, junction to case (θ_{jc})			0.1°C/MW
Output voltage			5.5 V	Power Dissipation per gate (50% Duty Cycle, V _{CC} = +5v)	15		MW

ELECTRICAL CHARACTERISTICS

Characteristics at $V_{cc} = +5.0V$		Values at Required Temperatures			Units
		Symbol	-55°C	+25°C	
INPUT:					
Input Load Current @ $V_{IN} =$ Other Inputs	I_L	1.33 0 4.5	1.33 0 4.5	1.33 0 4.5	mA Max. Volts Volts
Input Leakage Current @ $V_{IN} =$ Other Inputs	$I_{IN\ LK}$	0.1 4.5 0	0.1 4.5 0	0.1 4.5 0	mA Max. Volts Volts
Inverse Beta Current @ $V_{IN} =$ Other Inputs	B_{INV}	0.1 4.5 Open	0.1 4.5 Open	0.1 4.5 Open	mA Max. Volts
Input (OFF Level) Breakdown Voltage @ $I_{IN} =$ Other Inputs	$BV_{IN}\ "1"$	5.5 1.0 0	5.5 1.0 0	5.5 1.0 0	Volts Min. mA Volts
Input (ON Level) Breakdown Voltage @ $I_{IN} =$ Other Inputs	$BV_{IN}\ "0"$	5.5 1.0 Open	5.5 1.0 Open	5.5 1.0 Open	Volts Min. mA
Logic "1" Threshold Voltage $V_{OUT} =$ $I_{OUT}\ (SG-40)$ $I_{OUT}\ (SG-41)$	$V_{TH}\ "1"$	2.0 0.45 20 10	1.7 0.45 20 10	1.4 0.45 20 10	Volts Volts Max. mA mA
Logic "0" Threshold Voltage $V_{OUT} =$ $I_{OUT}\ (SG-40)$ $I_{OUT}\ (SG-41)$	$V_{TH}\ "0"$	1.0 2.5 1.5 0.7	1.2 2.4 1.5 0.7	0.9 2.7 1.5 0.7	Volts Volts Min. mA mA
OUTPUT:					
Output Leakage Current @ $V_{OUT} =$ Inputs	$I_{O\ LK}$	0.25 5.5 0	0.25 5.5 0	0.25 5.5 0	mA Max. Volts Volts
Output Short Circuit Current @ Input	I_{SC}	10 45 0	10 45 0	10 45 0	mA Min. mA Max. Volts
Logic "0" Level @ $V_{IN} =$ $I_{OUT}\ (SG-40)$ $I_{OUT}\ (SG-41)$	Logic "0"	0.40 2.8 20 10	0.40 2.8 20 10	0.45 2.8 20 10	Volts Max. Volts mA mA
Logic "1" Level @ $V_{IN} =$ $I_{OUT}\ (SG-40)$ $I_{OUT}\ (SG-41)$	Logic "1"	2.8 0.45 1.5 0.7	3.2 0.45 1.5 0.7	3.35 0.45 1.5 0.7	Volts Min. Volts mA mA
POWER REQUIREMENTS:					
Breakdown Voltage @ $I_{cc} =$ Inputs	BV		8.0 10 0		Volts Min. mA Volts
"ON" State Current Drain Inputs	$I_{cc\ 0}$	12 Open	12 Open	12 Open	mA Max.
"OFF" State Current Drain Inputs	$I_{cc\ 1}$	6 0	6 0	6 0	mA Max. Volts

Fig. No.

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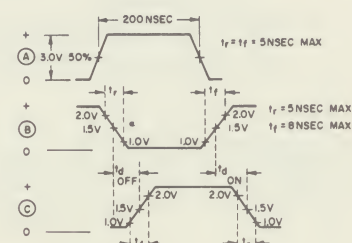
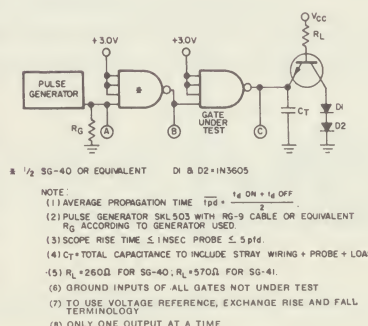
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SWITCHING

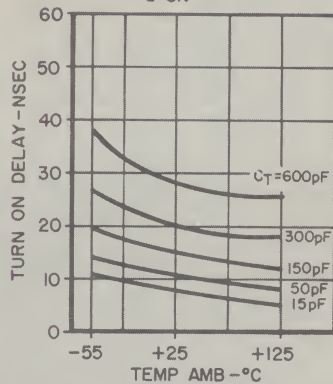
SWITCHING CHARACTERISTICS	CONDITIONS		LIMITS	
	V _{CC} volts	T _A °C	FANOUT	C _T TIME — nsec
			SG-40	SG-41
Turn On Delay	+5.0	+25	15	7
Turn Off Delay			15	7
Rise Time Note 7			15	7
Fall Time Note 7			15	7



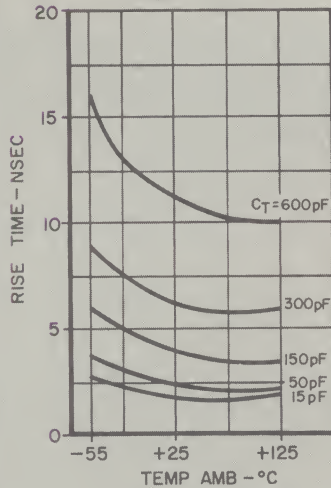
TYPICAL SWITCHING CHARACTERISTICS $V_{CC} = +5.0V$

FAN OUT = 1

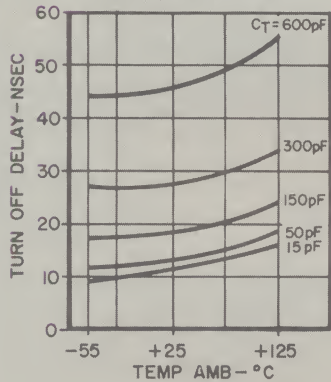
T_d ON VS TEMP



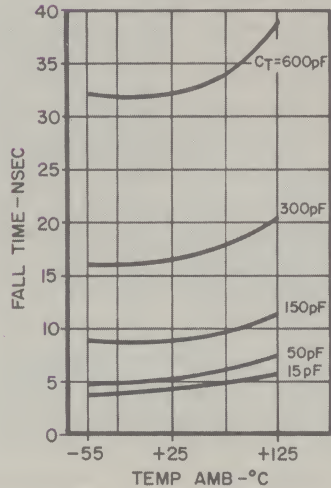
T_{RISE} VS TEMP



T_d OFF VS TEMP

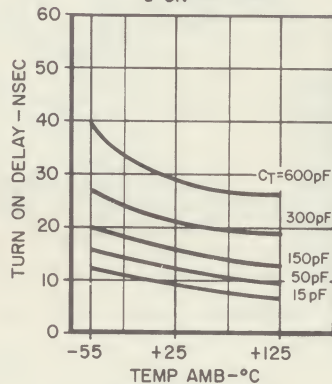


T_{FALL} VS TEMP

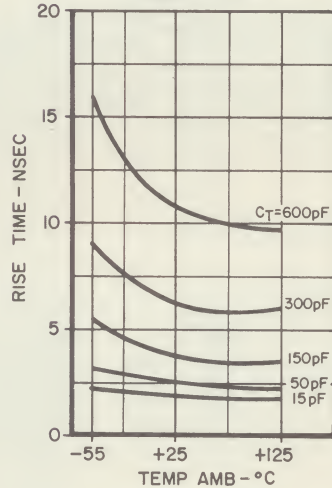


FAN OUT = 7

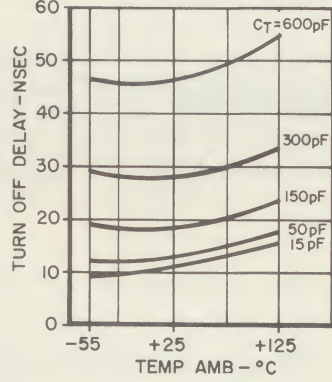
T_d ON VS TEMP



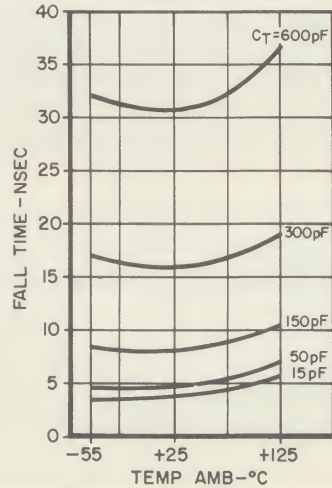
T_{RISE} VS TEMP



T_d OFF VS TEMP

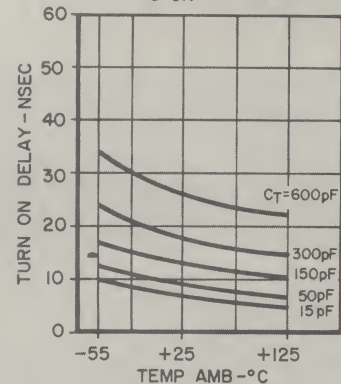


T_{FALL} VS TEMP

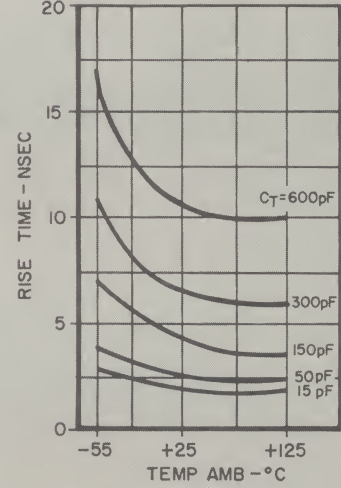


FAN OUT = 15

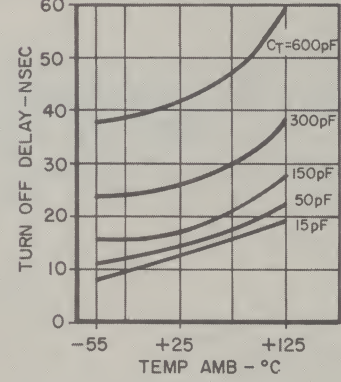
T_d ON VS TEMP



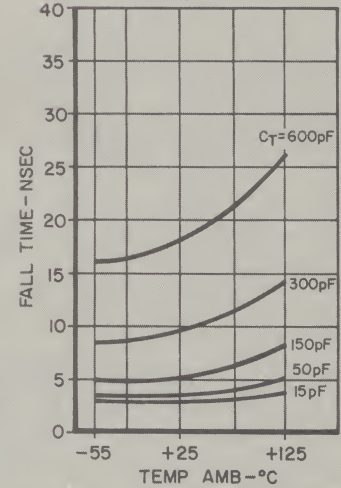
T_{RISE} VS TEMP



T_d OFF VS TEMP



T_{FALL} VS TEMP



RATINGS

Min. Typical Max.

Min. Typical

Max.

VOLTAGE				TEMPERATURE AND POWER			
Supply voltage (D.C.)			8.0 V _{DC}	Operating	-55		+125°C
Supply voltage (surge, 1 sec)			12.0 V	Storage	-65		+200°C
Supply voltage (operating)	4.5	5.0	6.0 V	Thermal gradient, junction to air (θ_{ja})			0.3°C/MW
Input voltage			5.5 V	Thermal gradient, junction to case (θ_{jc})			0.1°C/MW
Output voltage			5.5 V	Power Dissipation per gate (50% Duty Cycle, V _{CC} = +5v)	15		MW

ELECTRICAL CHARACTERISTICS

Characteristics at $V_{cc} = +5.0V$		Values at Required Temperatures			Units
		Symbol	-55°C	+25°C	
INPUT:					
Input Load Current @ $V_{IN} =$ Other Inputs	I_L	1.33 0 4.5	1.33 0 4.5	1.33 0 4.5	mA Max. Volts Volts
Input Leakage Current @ $V_{IN} =$ Other Inputs	$I_{IN LK}$	0.1 4.5 0	0.1 4.5 0	0.1 4.5 0	mA Max. Volts Volts
Inverse Beta Current @ $V_{IN} =$ Other Inputs	B_{INV}	0.1 4.5 Open	0.1 4.5 Open	0.1 4.5 Open	mA Max. Volts Volts
Input (OFF Level) Breakdown Voltage @ $I_{IN} =$ Other Inputs	$BV_{IN} "1"$	5.5 1.0 0	5.5 1.0 0	5.5 1.0 0	Volts Min. mA Volts
Input (ON Level) Breakdown Voltage @ $I_{IN} =$ Other Inputs	$BV_{IN} "0"$	5.5 1.0 Open	5.5 1.0 Open	5.5 1.0 Open	Volts Min. mA Volts
Logic "1" Threshold Voltage $V_{OUT} =$ $I_{OUT} (SG-40)$ $I_{OUT} (SG-41)$	$V_{TH} "1"$	2.0 0.45 20 10	1.7 0.45 20 10	1.4 0.45 20 10	Volts Volts Max. mA mA
Logic "0" Threshold Voltage $V_{OUT} =$ $I_{OUT} (SG-40)$ $I_{OUT} (SG-41)$	$V_{TH} "0"$	1.0 2.5 1.5 0.7	1.2 2.4 1.5 0.7	0.9 2.7 1.5 0.7	Volts Volts Min. mA mA
OUTPUT:					
Output Leakage Current @ $V_{OUT} =$ Inputs	$I_{O LK}$	0.25 5.5 0	0.25 5.5 0	0.25 5.5 0	mA Max. Volts Volts
Output Short Circuit Current @ Input	I_{SC}	10 45 0	10 45 0	10 45 0	mA Min. mA Max. Volts
Logic "0" Level @ $V_{IN} =$ $I_{OUT} (SG-40)$ $I_{OUT} (SG-41)$	Logic "0"	0.40 2.8 20 10	0.40 2.8 20 10	0.45 2.8 20 10	Volts Max. Volts mA mA
Logic "1" Level @ $V_{IN} =$ $I_{OUT} (SG-40)$ $I_{OUT} (SG-41)$	Logic "1"	2.8 0.45 1.5 0.7	3.2 0.45 1.5 0.7	3.35 0.45 1.5 0.7	Volts Min. Volts mA mA
POWER REQUIREMENTS:					
Breakdown Voltage @ $I_{cc} =$ Inputs	BV		8.0 10 0		Volts Min. mA Volts
"ON" State Current Drain Inputs	$I_{cc 0}$	12 Open	12 Open	12 Open	mA Max.
"OFF" State Current Drain Inputs	$I_{cc 1}$	6 0	6 0	6 0	mA Max. Volts

Fig. No.

1

2

3

2

3

8

9

5

7

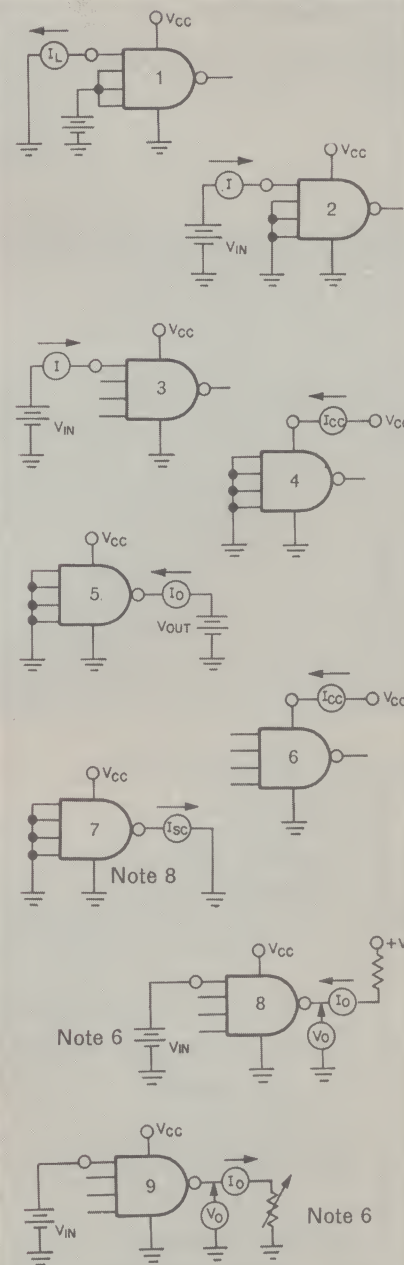
8

9

4

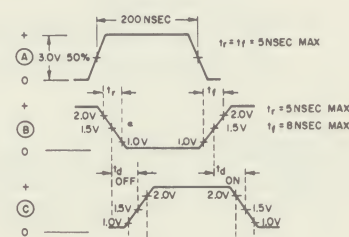
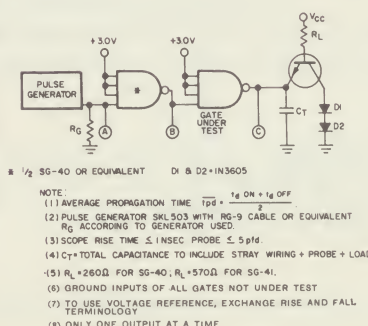
6

4



SWITCHING

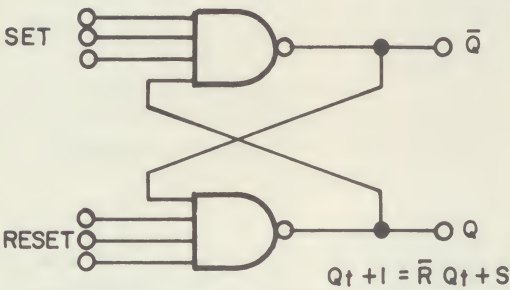
	CONDITIONS		LIMITS	
	V _{CC} volts	T _A °C	FANOUT	C _T TIME — nsec
			SG-40	SG-41
Turn On Delay	+5.0	+25	15	7
Turn Off Delay			15	7
Rise Time Note 7			15	7
Fall Time Note 7			15	7



APPLICATION no. 1.

Using the SG40 series NAND gates, a set reset flip-flop can be constructed. Set and reset terminals must be activated.

SET RESET FLIP FLOP
USING DUAL 4 INPUT NAND GATES

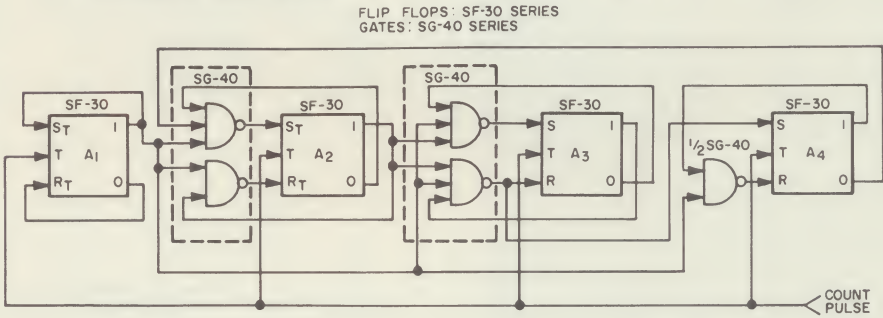


↑		↑ _{n+1}
R	S	Q
0	0	Q _t
0	1	1
1	0	0
1	1	NA

APPLICATION no. 2.

Using SG40 series gates, having four inputs, functions such as the synchronous Binary Decade counter can be readily implemented. Having dual gates in one package reduces the "can count" and simplifies wiring. Total power for the system is approximately 220 mw. Counting speed approximately 5 megacycles.

SYNCHRONOUS BINARY DECADE (BCD) COUNTER-S.R.T. FLIP FLOP (8-4-2-1' CODE)



- SET A₁ = Q₁

SET A₂ = Q₁ Q₂ Q₄

SET A₃ = Q₁ Q₂ Q₃

SET A₄ = Q₁ Q₂ Q₃
- RESET A₁ = Q₁

RESET A₂ = Q₁ Q₂

RESET A₃ = Q₁ Q₂ Q₃

RESET A₄ = Q₁ Q₄

A ₄	A ₃	A ₂	A ₁	DECIMAL EQUIV.
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

TYPICAL V_{IN}-V_{OUT} TRANSFER CHARACTERISTIC
-55°C TO +125°C

